

R15

Code No: 124AF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, May - 2017

**DIGITAL DESIGN USING VERILOG HDL**  
(Electronics and Communication Engineering)

Time: 3 Hours

Max. Marks: 75

**Note:** This question paper contains two parts A and B.  
Part A is compulsory which carries 25 marks. Answer all questions in Part A.  
Part B consists of 5 Units. Answer any one full question from each unit.  
Each question carries 10 marks and may have a, b, c as sub questions.

**PART-A**

(25 Marks)

- 1.a) Write a short note on keywords. [2]
- b) Write about white space character with an example. [3]
- c) Illustrate an example to design tri type net. [2]
- d) Explain the gate Delay. [3]
- e) What are local variables? [2]
- f) Write about 'Repeat' Construct. [3]
- g) Define Computer Directives. [2]
- h) Define time delay with example. [3]
- i) Write about switch primitives. [2]
- j) Draw the basic RAM Cell Diagram. [3]

**PART-B**

(50 Marks)

- 2.a) Explain in detail the Levels of Design Description. [5+5]
  - b) Explain the concept of numbers in Language constructs. [5+5]
- OR**
- 3.a) Explain the Strings with suitable examples. [5+5]
  - b) Explain the Simulation and Synthesis in Verilog HDL. [5+5]
- 4.a) Describe the model structures with an example. [5+5]
  - b) Design a 3 to 8 decoder. [5+5]
- OR**
- 5.a) Discuss the tri state gates with an example. [5+5]
  - b) Write about array of instances of primitives. [5+5]
- 6.a) Explain with an example how 'while' construct is used. [5+5]
  - b) Write briefly about functional bifurcation. [5+5]
- OR**
- 7.a) Design an 8-bit adder module using for loop. [5+5]
  - b) Explain disable construct with an example. [5+5]

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- 8.a) Discuss Basic Transistor Switches.
- b) Explain File Based Tasks and Functions. [5+5]

**OR**

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- 9.a) Explain the Strength Contention with Trireg Nets. [5+5]
- b) Explain the Hierarchical Access.

- 10.a) Explain the Sequential Model-Feedback Model.
- b) Write about Assertion Verification. [5+5]

**OR**

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- 11.a) Explain the Static Machine Coding.
- b) Explain the Sequential Circuit Testing. [5+5]

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