

R13

Code No: 113BU

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, December-2014

SWITCHING THEORY AND LOGIC DESIGN

(Common to ECE, EIE)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

Part- A**(25 Marks)**

- 1.a) What do you mean by self complementing codes. Give two examples. [2M]
b) State and prove consensus theorem. [3M]
c) What is a standard POS form? [2M]
d) How does the look-ahead-carry adder speed up the addition process? Why serial adders are slower than parallel adders? [3M]
e) What are preset and clear inputs? [2M]
f) Distinguish between combinational and sequential switching circuits. [3M]
g) What are the applications of counters? [2M]
h) What is a twisted ring counter? [3M]
i) What is a Mealy machine? [2M]
j) What is a merger graph? [3M]

Part-B**(50 Marks)**

- 2.a) What is Hamming code? How is the Hamming code word tested and corrected?
b) Perform the decimal addition of $679.6 + 536.8$ in the 8421 code.

OR

- 3.a) Obtain the duals of the following functions:
i) $\overline{X}YZ + X\overline{Y}Z + XY\overline{Z} + X\overline{Y}Z$
ii) $\overline{A}BC + \overline{A}BC + \overline{A}BC + \overline{A}BC$
b) Realize XOR function using AOI logic and NAND logic.

- 4.a) Realize a full adder using only 2-input NAND gates.
b) Implement the following logic function using an 8:1 MUX.
 $F(x, y, z) = \sum m(0, 2, 3, 5)$

OR

- 5.a) Minimize the following multiple output functions using K-maps.
 $f_1 = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 4, 5, 14, 15)$
 $f_2 = \sum m(1, 2, 6, 7, 8, 13, 14, 15) + d(3, 5, 12)$
b) Draw the logic diagram of a 1-line to 4-line demultiplexer and explain its working.
- 6.a) Draw the logic diagram of a master slave JK flip flop using NAND gates and explain its truth table.
b) Define the following terms as applied to flip flops.
(i) Set-up time, (ii) Hold time, (iii) Propagation delay time.

OR

- 7.a) Explain the conversion of SR flip flop to JK flip flop.
b) Obtain the characteristic equations of SR and JK flip flops.

- 8.a) Draw the diagram of mod-10 Asynchronous counter using T-flip flops and explain its working.
- b) Draw the logic diagram of a 4-bit ring counter using JK flip flops and explain its working.

OR

9. Design a Synchronous modulo-6 gray code counter using T-flip flops.
- 10.a) What is a Merger graph?
- b) Draw the Merger graph and obtain the set of maximal compatibles for the incompletely specified sequential machine whose state table is given in Table 1.

PS	NS, Z	
	I ₁	I ₂
A	E, 0	D, 1
B	F, 0	D, 0
C	E, —	B, 1
D	F, 1	B, 0
E	C, 1	F, 1
F	D, —	C, 0

OR

- 11.a) Draw the ASM chart of a Binary multiplier.
- b) Obtain the control subsystem of a binary multiplier using logic gates.

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